	US ATLAS HL-LHC Upgrade BASIS of ESTIMATE (BoE)	**Date of Est:** 16 Nov 2015
		Prepared by: Elliot Lipeles
		Docdb #:
WBS number: 6.8.y.3	**WBS Title: L1Global Hadronic Triggering Firmware**	

WBS Dictionary Definition:
L1Global hadronic triggering firmware, includes algorithm implementation for topological clustering, jet-finding, fat-jet identification, global quantity reconstruction, and the use of tracking information in pile-up rejection.

Estimate Type (check all that apply – see BOE Report for estimate type by activity):

___ Work Complete
___ Existing Purchase Order
___ Catalog Listing or Industrial Construction Database
___ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications
_x_ Engineering Estimate based on Similar Items or Procedures
___ Engineering Estimate based on Analysis
___ Expert Opinion

Supporting Documents (including but not limited to):

Details of the Base Estimate (explanation of the Work)

The L1Global system will take as inputs the regional tracking information from L1Track and full granularity calorimeter information. The L1Global will support a wide variety trigger object reconstruction. This BoE addresses a plan for the hadronic triggering which includes:
– Topological clustering similar to offline
– Hadronic calorimeter object reconstruction
  – Jet finding
  – Fat-jet identification
  – Global quantity reconstruction including: MET, HT, MHT and jets-without-jets
– Track-based pile-up rejection for 4-jet triggers and HT/MHT quantities

Effort: The firmware development will follow two phases a preproduction phase using demonstrator boards followed by a second phase on the hardware selected/developed for the event processor boards. The manpower required for the development of each algorithm is assumed to be 2 FTEs distributed over 4 years(*EL*, how do we define the profile? Stretch to the 6 years 2019-25 in the scoping Gantt chart? … that seems extended) based on the

experience developing the gFEX firmware for Phase-1. Because the Topological clustering algorithm involves iterative processes for which the gFEX experience is less applicable, it is expected to required more effort and is instead assigned 4 FTEs.

Engineering cost is assumed to be $100/hour full loaded. This is consistent with the higher of the two institute costs of the gFex firmware development (which are two of the planned contributing institutes) and the middle of the range of costs obtained from two other institutions. This is assumed to be a 2015 number and 3%/year of inflation is assumed.

Material: For each institute we assume: $5k to cover firmware license fees, $2k to cover a development board, $25k is assumed to cover access to a production board and a test crate. The testboards may be more expensive than the $25k in which case institutes would need to coordinate sharing 2-3 test stands.

Travel: Two trip to workshops :one early in the development cycle and one at the start of preproduction, and two trips to CERN for integration tests. Each trip has an assumed cost of $2.5k.

The time profile target is defined to have the full firmware package complete at the start of LS3, so that LS3 can be used as a commissioning period.

	Labor Hrs	Labor $	M&S $	Travel $	Grand Total $
6.8.y.3 WBS Title	21,120	$2,271,638	$222,000	$60,000	$2,553,638
Topoclustering					
Engineer	7120	$757,213	$75,000	$20000	$851,213
Jet Finding					
Engineer	3560	$378,606	$37000	$10000	$425,606
Fat-jet Reconstruction					
Engineer	3560	$378,606	$37000	$10000	$425,606
Global Quantities					
Engineer	3560	$378,606	$37000	$10000	$425,606
Track-based pile-up rejection					
Engineer	3560	$378,606	$37000	$10000	$425,606

Table 1: L1 Global Firmware from Chicago, Indiana, LSU, MSU, Oregon, and Pitt

Assumptions:

- L1 Global boards will be some admixture of FPGA and GPU where a demonstrator board or boards relevant to the particular algorithm can be found
- Full L1 Global prototype boards are available in FY2021 at the time of the expect full design review

Risk Analysis

- Schedule Risk – Probability: *low*, Impact: *low*, Overall: *low*
    - Potential Problem: Development boards are not available for the selected hardware

  Mitigation: Then we would need to move directly to using a prototype board which could delay the start of the development

- Cost Risk – Probability: medium, Impact: low , Overall: low
    - Potential Problem: Algorithms are more complex that expected of additional algorithms are needed as the understanding of the pile-up advances
    - Mitigation: gFEX experience suggests that the cost increases would be moderate.

- Technical/Scope Risk – Probability: medium, Impact: low, Overall: low
    - Potential Problem: Algorithms are more complex that expected of additional algorithms are needed as the understanding of the pile-up advances
    - Mitigation: This would have an incremental effect on the cost

- External Risk – Probability: medium, Impact: low, Overall: low
    - Potential Problem: At each step, delays in the event processor selection and production could delay the development cycle
    - Mitigation: The overall schedule has enough float that reasonable delays (6-12 months) can be accomadated

Contingency Analysis

Will be done separately

Comments:

Quotes also go here